REMARKS/ARGUMENTS

Claims 1-29 are pending the present patent application. Claims 3, 8-10, 21, 23, and 27 have been amended. No new matter has been added to the amended claims. Reconsideration of the claims is respectfully requested.

The Rejections Based on § 112, Second Paragraph

Claims 1, 11, 21, and 28 were rejected for purportedly omitting essential structural cooperative relationships of elements, amounting to a gap between necessary structural connections. Specifically, the office action stated that the element "programmable logic portion" lacks a structural cooperative relationship with the first and the second JTAG circuits.

The office action cites MPEP § 2172.01, which states that "a claim which fails to interrelate *essential elements* of the invention as defined by applicant(s) in the specification may be rejected under 35 U.S.C. § 112, second paragraph, for failure to point out and distinctly claim the invention."

The specification of the present application does not state that the programmable logic portion is an essential element of all embodiments of the invention.

For example, the specification of the present application states that "Embedded logic which includes a processor may be added to a chip that contains a programmable logic portion. In *one embodiment of the present invention*, the functionality of JTAG circuitry that is part of the control logic associated with the programmable logic portion of the chip may be augmented by adding JTAG mirroring circuitry of the present invention to the embedded logic portion of the chip." Page 2, lines 29-33. Also, claim 27 is an independent claim that does not recite a programmable logic portion.

MPEP § 2172.01 cites Ex Parte Nolden 149 U.S.P.Q. 378 (Bd. Pat. App. 1965), which states that "it is not essential to a patentable combination that there be interdependency between the elements of the claimed device or that the elements operate concurrently toward the desired result."

For these reasons, it is submitted that claims 1, 11, 21, and 28 satisfy the legal requirements of 35 U.S.C. § 112, second paragraph.

The Prior Art Rejections

Claims 1-29 were rejected as being anticipated by U.S. patent 5,768,288 to Jones. Applicants respectively disagree with this rejection.

1. **Claims 1, 11, and 21**

Claims 1, 11, and 21 recite an integrated circuit or chip that includes a processor, a programmable logic portion, and two JTAG circuits.

The Jones patent does not disclose or suggest placing a processor, a programmable logic portion, and two JTAG circuits all on *a single integrated circuit or chip*.

In the Jones patent, "Device under test 400 may be a single integrated circuit device or a system on a PCB." Column 6, lines 35-37.

Along these lines, Figure 4b in Jones does not disclose that devices under test 430 and device under test 446 are together part of one single integrated circuit. In addition, Figure 24 of Jones does not disclose that device under test 2408 and DSP 2402 are both part of one single integrated circuit.

It would not have been obvious based on the Jones patent to provide a processor, a programmable logic portion, and two JTAG circuits all on a single integrated circuit or chip. Jones provides no motivation to combine a processor with a programmable logic device. In Figure 24 of Jones, for example, DSP 2402 and DUT 2408 are shown as separate chips.

Also, each device under test shown in Jones appears to have a single test circuit. Therefore, Jones provides no motivation to place two JTAG test circuits on a single integrated circuit.

For these reasons, it is respectfully submitted that claims 1, 11, 21, and their dependent claims are novel and nonobvious over the cited prior art references.

2. **Claim 27**

Claim 27 recites an integrated circuit that includes a processor, a first JTAG circuit with a first plurality of data registers, and a second JTAG circuit with a second plurality of data registers. Claim 27 has been amended to recite "wherein the second plurality of data

registers are designed to perform functions that are not performed by the first plurality of data registers."

Page 2, lines 21-25, page 9, lines 5-7; and Figures 7 and 8 of the present application provide support for this amendment. Figures 7 and 8 illustrate two JTAG circuits with data registers that perform different functions. According to this embodiment of the present invention, the second JTAG circuit is designed to augment the debugging functionality of the first JTAG circuit.

Jones does not disclose or suggest these features of amended claim 27. For example, Jones does not suggest that data registers in test circuit 434 are designed to perform functions that are not performed by data registers in test circuit 450.

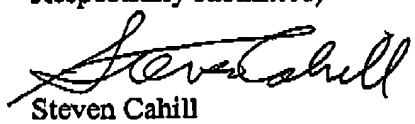
For these reasons, it is respectfully submitted that amended claim 27 and its dependent claims are novel and nonobvious over the Jones patent.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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